<u>In the Claims</u>:

1.-111. (Canceled)

112. (Original) An integrated circuit system, comprising:

a first integrated circuit chip that is configured to generate data and strobe signals at outputs thereof; and

a second integrated circuit chip that receives the data and strobe signals and latches a buffered version of the data signal in-sync with leading edges of a pair of complementary strobe signals that are derived from a delayed timing signal, said second integrated circuit chip having a delay device therein that comprises a digital delay line having a plurality of injection ports, said digital delay line configured to generate the delayed timing signal by adding at least a percent-of-clock period delay to a timing signal that is derived from the strobe signal and accepted at an enabled one of the plurality of injection ports of the digital delay line, and further configured to be responsive to an injection control signal having a value that sets a length of the delay by specifying a location of the enabled one of the plurality of injection ports.

113. (Original) The integrated circuit system of Claim 112, wherein said delay device is responsive to a system clock signal having a period that sets the length of the period from which the percent-of-clock period delay is measured; and wherein said first integrated circuit chip is responsive to a buffered version of the system clock signal.

114. (Original) The integrated circuit system of Claim 113, wherein said first integrated circuit chip comprises a delay locked loop that receives the buffered version of the system clock signal.

115. (Original) The integrated circuit system of Claim 112, wherein said first integrated circuit chip comprises a dual data rate (DDR) memory device.

116. (Original) The integrated circuit system of Claim 115, wherein the dual data rate (DDR) memory device is a DDR FIFO, said DDR FIFO comprising a plurality of memory devices that are configured to support any combination of dual data rate (DDR) or

single data rate (SDR) write modes that operate in-sync with a write clock signal and DDR or SDR read modes that operate in-sync with a read clock signal.

117. (Original) An integrated circuit system, comprising:

a dual data rate (DDR) memory chip that is configured to generate a DDR data signal and a DQS strobe signal at respective outputs thereof; and

a DDR memory controller that receives the DDR data signal and the DQS strobe signal and captures a buffered version of the DDR data signal at a bandwidth of greater than about 200 Mwords/sec and in-sync with leading edges of a pair of complementary strobe signals that are derived from a delayed DQS strobe signal, said DDR memory controller having a digital delay line therein that is configured to generate the delayed DQS strobe signal by adding at least a percent-of-clock period delay to a buffered version of the received DQS strobe signal, and is further configured to be responsive to a multi-bit injection control signal having a value that sets a length of the delay.

118. (Original) The integrated circuit system of Claim 117, wherein the buffered version of the received DQS strobe signal is accepted at an enabled one of a plurality of injection ports of the digital delay line; and wherein the multi-bit injection control signal sets the length of the delay by specifying a location of the enabled one of the plurality of injection ports.

119. (Original) The integrated circuit system of Claim 117, wherein the digital delay line comprises a string of delay elements therein that are electrically coupled to a first bias signal line; and wherein said DDR memory controller comprises a first bias signal generator that is configured to intermittently pump the first bias signal line with displacement current.

120. (Original) The integrated circuit system of Claim 117, wherein the digital delay line comprises a string of delay elements therein that are electrically coupled to a first bias signal line; and wherein said DDR memory controller comprises a first bias signal generator that is configured to float the first bias signal line at a first voltage level when the string of delay elements are active.

121. (Original) The integrated circuit system of Claim 120, the first bias signal generator is further configured to intermittently pump the first bias signal line with displacement current when the string of delay elements is inactive.

122. (Original) An integrated circuit system, comprising:

a dual data rate (DDR) memory chip that is configured to generate a DDR data signal and a DQS strobe signal having a frequency of about 133 MHz at respective outputs thereof; and

a DDR memory controller that receives the DDR data signal and the DQS strobe signal and is configured to capture a buffered version of the DDR data signal at a bandwidth of about 266 Mwords/sec and in-sync with leading edges of a pair of complementary strobe signals that are derived from a delayed DQS strobe signal, said DDR memory controller having a digital delay line therein that is configured to generate the delayed DQS strobe signal by adding about a twenty percent-of-clock period delay to a buffered version of the DQS strobe signal.

123. (Original) The integrated circuit system of Claim 122, wherein a data valid window associated with the buffered version of the DDR data signal at the time of capture is in a range between about 1.6 ns and about 1.65 ns.

124. (Original) The integrated circuit system of Claim 123, wherein a delay error margin associated with the digital delay line is no greater than about ±0.2 ns over rated ranges of temperature and power supply voltage variations.

125. (Original) The integrated circuit system of Claim 122, wherein a delay error margin associated with the digital delay line is no greater than about ±0.2 ns over rated ranges of temperature and power supply voltage variations.

126. (Original) The integrated circuit system of Claim 122, wherein the digital delay line comprises a string of delay elements therein that are electrically coupled to a first bias signal line; and wherein said DDR memory controller comprises a first bias signal generator that is configured to intermittently pump the first bias signal line with displacement current.

127. (Original) The integrated circuit system of Claim 122, wherein the digital delay line comprises a string of delay elements therein that are electrically coupled to a first bias signal line; and wherein said DDR memory controller comprises a first bias signal generator that is configured to float the first bias signal line at a first voltage level when the string of delay elements are active.

128. (Original) The integrated circuit system of Claim 127, the first bias signal generator is further configured to intermittently pump the first bias signal line with displacement current when the string of delay elements is inactive.

129. (Original) The integrated circuit system of Claim 122, wherein a data valid window associated with the buffered version of the DDR data signal at the time of capture is in a range between about 1.55 ns and about 1.70 ns.

130.-134. (Canceled)

Respectfully submitted,

Grant J. Scott
Registration No. 36,925
Attorney for Applicants

USPTO Customer No. 20792
Myers Bigel Sibley & Sajovec
Post Office Box 37428
Raleigh, North Carolina 27627
Telephone: 919/854-1400

CERTIFICATE OF EXPRESS MAILING

Express Mail Label No. EV 318419992 US
Date of Deposit: August 18, 2003

I hereby certify that this correspondence is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR § 1.10 on the date indicated above and is addressed to: Mail Stop Patent Application, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Candi L. Riggs
Date of Signature: August 18, 2003